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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,190	12/05/2003	Gary L. Swoboda	TI-34669	2410

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,190	SWOBODA ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Swoboda et al., for "Apparatus and method for trace stream identification of a pause point in code execution sequence" filed December 5, 2003, has been examined.

Claims 1-11 are presented for examination.

Claims 1-11 are rejected under 35 USC § 102.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No.10728627. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

As per claim 1 of the instant application, claim 1 has the common limitation of

" timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus" with, claim 1 of 10728627. This common limitation performs the same function.

It would have been obvious to one of ordinary skill in the art at the time the invention to use the timing trace, the program counter trace, and the synchronization method of claim 1 of the instant application in the processing unit testing method of claim 1 of 10728627.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because according to the specifications of the instant application using the timing trace, the program counter trace, and the synchronization method is used to test a processing unit. Phillips et al. (U.S. Patent No. 5,321,828) discloses the use of the timing trace (col. 60, lines 56-60), the program counter trace (col. 31, lines 53-56), and the synchronization signals (Fig. 8B) and (Fig. 9, elements 204, 206) in testing of processing units.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Phillips et al. (U.S. Patent No. 5,321,828).

As per claim 1, Phillips discloses during the testing of the operation of processing unit (col. 21, lines 54-68), a system for identifying the occurrence of a pause point condition in the processing unit instruction execution (Fig. 11, *Breakpoint detection*) the system comprising:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream (col. 60, lines 56-60)

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream (col. 31, lines 53-56)

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals resulting in periodic sync markers in the timing trace stream and in the program counter trace stream (Fig. 8B) and (Fig. 9, elements 204, 206)

wherein the program counter trace apparatus is responsive to a pause point signal, the program counter trace apparatus generating a sync marker signal group identifying the occurrence of the pause point signal and relating the pause point signal (Fig. 11) to the timing trace stream and to the program code execution (Fig. 9, element 206).

As per claim 2, Phillips discloses the marker signal group includes a program counter address, a timing index and a periodic sync ID (col. 31, lines 53-56) and (Fig. 9, elements 204, 206).

As per claim 3, Phillips discloses data trace apparatus responsive to signals from the processing unit, the data trace apparatus generating a data trace stream, wherein the periodic signals are applied to the data trace apparatus resulting in periodic sync markers in the data trace stream (col. 60, lines 56-60) and (col. 31, lines 53-56)

a host processing unit (col. 46, lines 46-48), the host processing unit responsive to the timing trace stream, the program counter trace stream and the data trace stream, the host processing unit reconstructing (col. 20, lines 44-46) the processing activity of the processing unit from the trace streams (col. 60, lines 56-60) and (col. 31, lines 53-56).

As per claim 4, Phillips discloses the method for communicating an occurrence of a pause point in instruction execution of a target processor unit to a host processing unit, the method comprising:

generating a timing trace stream (col. 60, lines 56-60)

a program counter trace stream (col. 31, lines 53-56), and data trace stream, and in the program counter trace stream, including a program pause point sync marker signal group indicating an occurrence of a pause point signal (Fig. 11, *Breakpoint detection*) and relating the signal occurrence to the data trace stream and to the timing trace stream (Fig. 9, elements 204, 206).

As per claim 5, Phillips discloses including periodic sync markers in the timing trace stream (Fig. 9, elements 204, 206) and in the program counter trace stream; and including in the pause point sync marker reference to a periodic sync marker (Fig. 11, *Breakpoint detection*).

As per claim 6, Phillips discloses in a processing unit test environment wherein a target processor (Fig. 1, element 26) transmits a plurality of trace streams to a host processing unit (col. 46, lines 46-48), a pause point sync marker signal group in a trace signal stream (Fig. 11, *Breakpoint detection*); the marker signal group comprising: indicia of the occurrence of a pause point signal (Fig. 11, *Breakpoint detection*); indicia of the relationship of the occurrence of the pause point signal to the target processor clock (Fig. 8A); and indicia of the relationship of the occurrence of the pause point

signal to the target processor program execution (col. 20, lines 15-27).

As per claim 7, Phillips discloses in a target processing unit (Fig. 1, element 26) generating trace test signals for transfer to a host processing unit (col. 46, lines 46-48), a program counter trace generation apparatus comprising: sync marker assembly apparatus (col. 31, lines 53-56), the sync marker assembly apparatus including:

a storage unit (col. 20, lines 30-46)

a decoder unit responsive to a pause point signal for storing an indicia of the pause point signal in the storage unit, the decoder unit generating a control signal (col. 8, lines 23-26)

a gate unit having a timing index, a periodic sync signal, and a program counter address, the gate unit storing the timing index (Fig. 8B), the periodic sync signal and the program counter address in the storage unit in response to the control signal (Fig. 7, element 62) and a FIFO unit, the storage unit transferring the stored signals to the FIFO unit in the form of a pause point sync marker (Fig. 7, element 62).

As per claim 8, Phillips discloses responsive to a selected control signal for transferring the pause point sync marker in the FIFO unit to an output port of the target processor (Fig. 7, element 62, 64).

As per claim 9, Phillips discloses the apparatus can form a periodic sync marker in response to a periodic sync signal (col. 20, lines 30-46).

As per claim 10, Phillips discloses the pause point signal indicates a suspension of instruction execution during a change from an original code sequence to a new code sequence (col. 27, lines 2-37).

As per claim 11, Phillips discloses the first instruction code sequence is one of an original interrupt service routine code or an original program code and the second instruction sequence is one of a new interrupt service routine and a new program code (col. 27, lines 2-37).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Shiell (U.S. Patent No. 6,041,176), "Emulation devices utilizing state machines".

Kashiwagi (U.S. Patent No. 4,780,819), "Emulator system utilizing a program counter and a latch coupled to an emulator memory for reducing fletch line of instructions stored in the emulator memory".

Oguma et al. (U.S. Patent No. 5,132,971), "In-circuit emulator".

Circello et al. (U.S. Patent No. 5,737,516), "Data processing system for performing a debug function and method therefor".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER